REMARKS/ARGUMENTS

In the Office Action, the Examiner rejected claims 1-5, 8-14, 16-18 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) and Surti et al. (US Patent No. 6,496,193). The Examiner stated in Paragraph 4, Page 3 of the outstanding Office Action that APA did not expressly teach the second tile converter of the present invention, but Surti taught it. The Applicant respectfully disagrees and traverses the rejections for the following reasons.

According to the present invention, two tile converters are provided. The first tile converter in communication with a graphics accelerator processes image data in linear mode into image data in a tile mode, which is stored in local memory. Image data from the core-logic unit in linear mode is converted into image data in tile mode by a second tile converter (or the second portion of a tile converting device of claim 10) and stored in system memory. The second tile converter or the second portion of the tile converting device is in communication with the core logic unit for converting the first image data outputted by the core logic unit in a linear mode into image data in a tile mode. The second tile converter is inherently disposed downstream of the core logic unit and independent from the microprocessor.

Both the APA and Surti disclose only one tile converting device or operation. Neither APA nor Surti discloses two tile converting devices as disclosed in the specification and recited in the claims. In addition, referring to Surti (col. 4, lines 23-38 and 58-61), Surti's conversion of host processor addresses to tile addresses is executed by the host processor which tiles the addresses first and then converts the tiled addresses to physical addresses. Therefore, Surti does not teach the second tile converter of the present invention which is disposed downstream of the core logic unit and independent from the microprocessor. Because all of the claim limitations are not taught or suggested by the combination of APA and Surti, the present invention would not have been obvious from the cited references.

As recited in the specification, paragraph [0005], an object of the invention is to provide a personal computer system involving no software transformation operation from a linear mode to a tile mode so as to increase software speed. Thus, the invention utilizes hardware tile-converting architecture to free the processor from a software transformation operation. However,

Surti's conversion of host processor addresses to tile addresses is executed by the host processor (col. 4, lines 62-63), which is inherently in a software manner. Claims 4, 5, 7, 13, 17, 18, 19, and 20 are drawn to the tile converters integrated into a logic chip, which feature is not taught by Surti. Therefore, Applicant respectfully submits that these claims would not have been obvious from the combined teachings of AAPA and Surti et al. because there is insufficient motivation to combine the AAPA with Surti et al. to arrive at the claimed invention. Withdrawal of the rejection is respectfully requested.

The examiner further rejected claims 6, 7, 15 and 19 under 35 USC 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA) and Surti et al. (US Patent No. 6,496,193) and Saxena et al. (US Patent Application No. 2003/0122837). As claims 6 and 7 are dependent from claim 1, claim 15 is dependent from claim 10, claim 19 is dependent from claim 17, and claims 1, 10 and 17 should be patentable according to the above discussion, claims 6, 7, 15 and 19 should also be patentable. Withdrawal of the rejection is respectfully requested.

In view of the foregoing remarks, allowance of all pending claims is respectfully requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If there are any remaining issues preventing allowance of the pending claims that may be clarified by telephone, the Examiner is requested to call the undersigned.

Respectfully submitted,

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